

Description

CONTROL SYSTEM WITH MULTIPROCESSOR ARCHITECTURE FOR AN INTERNAL COMBUSTION POWERTRAIN

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] The present application claims priority to Italian Patent Application Serial No. BO2003A 000256 filed April 30, 2003, the contents of which are incorporated herein by reference.

BACKGROUND OF INVENTION

FIELD OF THE INVENTION

[0002] The present invention relates to a control system with multiprocessor architecture for an internal combustion powertrain.

DESCRIPTION OF RELATED ART

[0003] Known powertrains comprise a control system that is ca-

pable of supervising the operation of the entire powertrain and comprises a single-processor computing unit having just one processor. In the great majority of cases, a powertrain manufacturer purchases the control system from an external supplier and requests said supplier to ensure that it is possible to implement control functions in the control system, which functions are intended for electronic devices produced by the powertrain manufacturer.

[0004] Typically, the producer of the control system tends to oversize the computing capacity and interconnectivity capacity of the computing unit in order to allow the engineers of the powertrain manufacturer to use the computing unit to implement control functions which they have developed themselves. However, the above-described solution of oversizing the computing capacity of a single-processor computing unit often proves inadequate in that execution of the control functions developed by the engineers of the powertrain manufacturer may interfere negatively with the execution of the powertrain control developed by the producer of the control system. Moreover, increasing the computing capacity of a single-processor computing unit can be achieved by modifying the internal architecture of the processor or by increasing the operat-

ing frequency of the processor itself; however, modifying the internal architecture of the processor is extremely costly, while increasing the operating frequency of the processor can complicate data exchange by means of existing buses that are designed to operate at a specific operating frequency.

[0005] U.S. Patent No. 5,367,665 A1 (issued November 22, 1994) discloses a multi-processor system for a motor vehicle and having at least two processors; the system carries out a first sequence of steps when power is switched on and, for a restart during operation, executes a second sequence of steps (the system distinguishes between power on and a restart and selects, the corresponding step sequence). In addition, a check is provided as to whether the number of resets of a processor has exceeded a pregiven threshold; in this case, a processor is transferred into the standby state for the operating cycle, which is then running.

[0006] U.S. Patent No. 5,454,095 A1 (issued September 26, 1995) discloses a multi-processor system, which has at least two processors jointly accessing the same memory and is useful for controlling processes of motor vehicles. The system memory is divided into at least two sectors, so as a

first processor accesses one memory sector only in the read mode and a second processor accesses it only in the write mode; the second processor accesses the other memory sector only in the read mode and the first processor accesses it only in the write mode. The processors are synchronized in such a way that the processors access the memory in the same way at the same time.

SUMMARY OF INVENTION

[0007] An object of the present invention is to provide a control system with multiprocessor architecture for an internal combustion powertrain, which does not have the above-described disadvantages and, in particular, is easily and economically implemented.

[0008] The present invention provides a control system with multiprocessor architecture for an internal combustion powertrain as recited in the attached claims.

BRIEF DESCRIPTION OF DRAWINGS

[0009] The present invention will now be described with reference to the attached drawings, which illustrate a non-limiting embodiment of the invention, in which: Figure 1 is a schematic diagram of an internal combustion powertrain equipped with the control system with multiproces-

sor architecture that is the subject matter of the present invention.

[0010] Figure 2 is a block diagram of the internal architecture of a computing unit of the control system of Figure 1.

DETAILED DESCRIPTION

[0011] In Figure 1, 1 denotes the overall internal combustion powertrain for a road vehicle (not shown); the powertrain 1 comprises an engine 2 equipped with four cylinders 3 (only one of which is shown in Figure 1), each of which is connected to an intake manifold 4 via a respective intake duct 5 controlled by at least one respective intake valve 6 and to an exhaust manifold 7 via a respective exhaust duct 8 controlled by at least one respective exhaust valve 9. The intake manifold 4 receives fresh air (i.e. air originating from the outside environment) via a throttle valve 10 that is adjustable between a closed position and a maximally open position; from the exhaust manifold 7 there leaves an exhaust device 11 equipped with one or more catalytic converters (not shown in detail) to discharge into the atmosphere the gases produced by combustion in the cylinders 3.

[0012] Four injectors 12 (one for each cylinder 3) are coupled to the respective intake ducts 5 in order to inject petrol

cyclically into said intake ducts 5; moreover, four spark plugs 13 (one for each cylinder 3) are coupled to the respective cylinders 3 in order cyclically to bring about ignition of the mixture present inside said cylinders 3.

[0013] Each cylinder 3 is coupled to a respective piston 14, which is capable of running linearly along the cylinder 3 and is mechanically connected to a powertrain crankshaft 15 by means of an associated connecting rod 16; in turn, the powertrain crankshaft 15 is mechanically connected to a gearbox 17 by means of an interposed clutch 18 in order to transmit drive torque to the drive wheels of the motor vehicle (not shown).

[0014] A control system 19 is associated with the powertrain 1, said system being capable of supervising the operation of the entire powertrain 1, i.e. the operation of the engine 2, clutch 18 and gearbox 17. The control system 19 comprises a computing unit 20 capable of executing both basic control functions of the powertrain 1 and ancillary control functions not directly related to the control of the powertrain 1. The basic control functions of the powertrain 1 are the control functions related to the production and transmission of drive torque, such as calculating and actuating the injection time, calculating and actuating the

ignition advance, monitoring the composition of the exhaust gases, actuating the clutch 18 and the gearbox 17. The ancillary control functions not directly related to the control of the powertrain 1 are control functions that are not implemented by the manufacturer of the control system 19 at the time of manufacture of the control system 19, but that may or may not be implemented by the manufacturer of the powertrain 1 after the manufacture of the control system 19. As shown in Figure 2, the computing unit 20 comprises a main processor 21 intended to execute basic control functions of the powertrain 1, at least one auxiliary processor 22 intended to execute ancillary control functions, a number of RAM type memories 23, a number of ROM type memories 24, a series of peripheral devices 25 of known type, a pair of peripheral bus connections 26 and 27 to which the peripheral devices 25 are connected in a known manner, and a main bus connection 28 through a cross-bar switch of the cross-bar bus type in order to allow the processors 21 and 22 to communicate with the memories 23 and 24 and with the peripheral bus connections 26 and 27 while avoiding the occurrence of conflicting communication operations by means of suitable access arbitration. According to an alternative

embodiment, not shown, the computing unit 20 comprises further auxiliary processors 22.

[0015] The computing unit 20 preferably comprises a single integrated circuit 29 that accommodates the processors 21 and 22, the memories 23 and 24, the main bus connection 28 and the peripheral bus connections 26 and 27, so providing an architecture generally known as "system on chip".

[0016] In general, the peripheral bus connection 26 is intended for connecting slow peripheral devices 25, such as "CAN", "SPI" and "TIMER UNIT" devices, while the peripheral bus connection 27 is intended for connecting high speed peripheral devices 25, such as "A/D CONVERTER" and "DMA" devices.

[0017] It is important to emphasize that the auxiliary processor 22 can execute inter-processor interrupt operations in order to wait for the main processor 21 to complete a particular computing algorithm; however, the opposite is not usually true, i.e. the main processor 21 should never have to wait for the auxiliary processor 22 to complete a particular computing algorithm. To state matters more clearly, it is theoretically possible for the main processor 21 to wait for the auxiliary processor 22 to complete a

particular computing algorithm by using an inter-processor interrupt operation, but this option should not be used in order to ensure that the execution of basic control functions of the powertrain 1 cannot in any way be slowed down by ancillary control functions.

[0018] In order to ensure optimum operation of the computing unit 20, the memories 23 and 24 may at least in part be protected: a first portion of the memories 23 and 24 is reserved for the main processor 21, and a second portion of the memories 23 and 24, different from the first portion, is reserved for the auxiliary processor 22.

[0019] From the above explanation, it is clear that the main processor 21 operates entirely autonomously with regard to the auxiliary processor 22, while the auxiliary processor 22 can operate either entirely autonomously with regard to the main processor 21 or dependently on the main processor 21. In this manner, the control system 19 is able to render the execution of the basic control functions of the powertrain 1 and of the ancillary control functions completely independent and parallel.

[0020] Finally, it is important to emphasise that at the time of manufacture of the control system 19, it is only the basic control functions of the powertrain 1 that are imple-

mented in the computing unit 20; the ancillary control functions may or may not be implemented in the computing unit 20 at another time by the manufacturer of the powertrain 1 or of the road vehicle (not illustrated) that accommodates the powertrain 1.

[0021] As a result of the many advantages offered by the above-described control system 19 for the powertrain 1, with multiprocessor architecture, said control system 19 can profitably be used for controlling any kind of internal combustion powertrain.

[0022] In particular, the control system 19 has great flexibility in the design of the control architecture, makes it readily feasible to integrate control functions implemented after the manufacture of the control system 19, and does not exhibit unwanted and/or uncontrolled interference between the basic control of the powertrain 1 and the control functions implemented after the production of the control system 19.